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09/708,795	11/07/2000	Stefanos Sidiropoulos	RB1-005US	2457

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EXAMINER	
CHANG, EDITH M	

ART UNIT	PAPER NUMBER
2634	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/708,795	Applicant(s) SIDIROPOULOS ET AL.	
	Examiner Edith M Chang	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-13,16-19,22-24,27-29,32-34,37-45,48,49,52-54 and 57-67* is/are rejected.

7)☒ Claim(s) *9,10,14,15,20,21,25,26,30,31,35,36,46,47,50,51,55 and 56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 18 recites the limitation "the reference voltages" in line 4 page 17. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 11-13, 16-19, 22-24, 27-29, 32-34, 37-45, 48-49, 52-54, and 57-67 are rejected under 35 U.S.C. 102(b) as being anticipated by Beers et al. (US 5578939).

Regarding **claims 1 & 39**, Beers et al. discloses an apparatus and its method comprising: a reference receiver (10 FIG.2) that receives an undistributed reference voltage (V2 FIG.3) and in response produce a buffered voltage (Vrecref FIG.3) that is derived at least in part from the undistributed reference voltage (FIG.7); signal receivers (16 FIG.2) associated respectively with a plurality of signal voltages (Vin from 24 FIG.2), wherein an individual signal receiver (FIG.11) receives both its associated signal voltage (Vin FIG.11) and the buffered voltage (Vrecref FIG.11), wherein the individual signal receiver evaluates its inputs and produce an output (Rout FIG.11).

Regarding **claims 2 & 40**, Beers et al. discloses the individual signal receiver evaluates by comparing (FIG.11 QN9 & QN10 perform the comparing) the associated signal voltage (Vin FIG.11) and the buffered voltage (Vrecref) to produce an output voltage.

Regarding **claims 3, 41, 62 & 67**, Beers et al. discloses the buffered voltage (Vrecref FIG.3) is the difference between the undistributed reference voltage (V2 FIG.3) and a distributed reference voltage (IRN FIG.3 where IRN from the current mirror 40 set by IRP which is provided by the differential amplifier DVA 34, column 5 lines 5-18, column 9 lines 60-65, i_2 provided by the difference of the V1 and V2 of 34 FIG.3 supplies the Vrecref).

Regarding **claims 4 & 42**, Beers et al. discloses the buffered voltage (Vrecref FIG.7) is proportional to the undistributed reference voltage (V2 FIG.7).

Regarding **claims 5, 43, 57, 61 & 66**, Beers et al. Beers et al. discloses the buffered voltage represents the noise of the signal voltages relative to the undistributed reference voltage (FIG.11 the noise of the signal voltages presents at the buffered voltage Vrecref related to the V2 FIG.7).

Regarding **claims 6-8 & 44-45**, Beers et al. discloses the reference receiver also receives a distributed reference voltage (IRN/IRP FIG.3 the distributed reference voltage, received as the drain of QN13 FIG.7) that is received by the signal receivers, wherein the reference receiver (10 FIG.3) is responsive to/compares the distributed reference voltage (IRN/IRP FIG.3) and the undistributed reference voltage (V2/Vrefline FIG.3) to produce the buffered voltage (Vrecref FIG.3), the buffered voltage representing the difference between the distributed reference voltage and the undistributed reference voltage (Vrecref represents the difference between the V2 and IRN/IRP FIG.3).

Regarding **claims 11-12, 22-23, 32-33 & 48-49**, Beer et al. discloses a plurality of signal buffers (14-16 FIG.2) that receive the signal voltages and in response produce buffered signal voltages; wherein the reference receiver and signal buffers are source-followers (FIG.7, FIG11).

Regarding **claims 13, 24 & 34**, Beer et al. discloses the reference reciver has a unity gain (where the Vrecref is not amplified by a gain).

Regarding **claims 16, 27 & 37**, Beer et al. discloses each signal voltage represents one of two values (column 2 lines 3-6 where the two values are presented, column 10 lines 45-55) and the signal receivers compare the buffered voltage (Vrecref FIG.11) and the signal voltages (Vin FIG.11) to determine the values represented by signal voltage (Rout FIG.11).

Regarding **claim 17**, Beer et al. discloses the reference voltage (the impedance of FIG.7) and the buffered voltage (the impedance of FIG.11) being subject to similar impedances.

Regarding **claims 18, 28, 38 & 52-53**, Beer et al. discloses the reference voltage (FIG.7 the input impedance of V2) and signal voltage being subject to similar impedances (FIG.11 the input impedance of Vin), wherein coupled signal noise is introduced approximately equally in the buffered voltage and the plurality of signal voltage, the approximately equal coupled signal noise being canceled in the evaluation performed by the signal receiver (Abstract, column 2 lines 13-30, the impedance is matched to reduce the noise).

Regarding **claim 19**, Beer et al. discloses an integrated circuit comprising: a reference input (V2 FIG.7) that receives a common reference voltage (V2/Vreline FIG.3); signal inputs (14-16 FIG.2) to receive signal voltages (Vin from 24 transmission line FIG.2), a reference buffer (10 FIG.2, 38 FIG.7) that receives the common reference voltage and in response produces a buffered reference voltage (Vrecref FIG.7); the signal comparators comparing

(FIG.11 QN9 & QN10 perform the comparing) the signal voltage (Vin FIG.11) and the buffered voltage (Vrecref) to produce an output voltage; wherein the reference voltage (FIG.7 the input impedance of V2) and signal voltage having similar impedances (FIG.11 the input impedance of Vin), wherein coupled signal noise is introduced approximately equally in the buffered voltage and the plurality of signal voltage, the approximately equal coupled signal noise being canceled performed by the signal comparator (Abstract, column 2 lines 13-30, the impedance is matched to reduce the noise).

Regarding **claim 29**, Beer et al. discloses a system comprising: a first integrated circuit that transmits a common reference voltage and signal voltages (20A/20B FIG.1, 20 FIG.2); a second integrated circuit (20B/20A FIG.1, 20 FIG.2) that receives the common reference voltage (Vreline FIG.3) and receive signal voltages (14-16 FIG.2, Vin from 24 FIG.2), having a reference buffer (10 FIG.2, 38 FIG.7) that receives the common reference voltage and in response produces a buffered reference voltage (Vrecref FIG.7); having the signal comparators comparing (FIG.11 QN9 & QN10 perform the comparing) the signal voltage (Vin FIG.11) and the buffered voltage (Vrecref) to produce an output voltage; wherein the reference voltage (FIG.7 the input impedance of V2) and signal voltage having similar impedances (FIG.11 the input impedance of Vin), wherein coupled signal noise is introduced approximately equally in the buffered voltage and the plurality of signal voltage, the approximately equal coupled signal noise being canceled performed by the signal comparator (Abstract, column 2 lines 13-30, the impedance is matched to reduce the noise).

Regarding **claims 54 & 58**, Beers et al. discloses an apparatus comprising: signal receivers (16 FIG.2) associated respectively with a plurality of signal voltages (Vin from 24

transmission line FIG.2), wherein an individual signal receiver (16 FIG.2, FIG.11) receives both its associated signal voltage (Vin FIG.2, FIG.11) and the buffered voltage (Vrecref FIG.2, FIG.11); wherein the individual signal receiver adjusts its inputs and produce an output (Rout FIG.11); a reference receiver (10 FIG.2) that receives an undistributed reference voltage (V2 FIG.3) and a distributed reference voltage (IRN/IRP FIG.3) to produce a buffered voltage (Vrecref FIG.3) that represents the difference between the undistributed reference voltage and the distributed reference voltage (IRN/IRP FIG.3 where IRN from the current mirror 40 set by IRP which is provided by the differential amplifier DVA 34, column 5 lines 5-18, column 9 lines 60-65, i_2 provided by the difference of the V1 and V2 of 34 FIG.3 supplies the Vrecref).

Regarding **claim 59**, Beers et al. discloses an integrated circuit comprising: two-stage receivers (20 FIG.2); a reference receiver (10 FIG.2) that receives both an undistributed reference voltage (V2 FIG.3) and a distributed reference voltage (IRN FIG.2); wherein the reference receiver compares the undistributed reference voltage and the distributed reference voltage to produce a buffered voltage (Vrecref FIG.2) wherein the first stage (14 FIG.2) of an individual signal receiver compares the signal voltage to the distributed reference voltage (IRN FIG.2 & FIG.10) to produce a voltage differential signal (COMP1/2 FIG.10, the 14->18 FIG.2); and the second stage (16 FIG.2) adjusts the voltage differential signal by the buffered voltage (18->16 FIG.2) to produce an output voltage (Rout FIG.11).

Regarding **claims 60 & 64**, Beers et al. discloses the two-stage receiver (20 FIG.2) has an input impedance similar to that of the reference receiver (10 FIG.2).

Regarding **claim 63**, Beers et al. discloses a system comprising a first integrated circuit that transmits a common reference voltage and signal voltages (20A/20B FIG.1, 20 FIG.2); a

second integrated circuit (20B/20A FIG.1, 20 FIG.2) that receives the common reference voltage (Vreline FIG.3) and receive signal voltages (14-16 FIG.2, Vin from 24 FIG.2); the second integrated circuit having a reference receiver (10 FIG.2) that receives the common reference voltage and in response produces a buffered reference voltage (Vrecref FIG.7); having two-stage signal receivers (20 FIG.2) adjusting one of the signal voltages by the buffered voltage(Vrecref FIG.2/FIG.10) to produce an output voltage (Rout FIG.10).

Regarding **claim 65**, Beer et al. discloses a reference receiver (10 FIG.2) that compares a distributed reference voltage (IRN FIG.2) to an undistributed reference voltage (V2 FIG.3) to produce a buffered voltage (Vrecref FIG.2); the first stage (14 FIG.2) of an individual signal receiver compares the signal voltage to the distributed reference voltage (IRN FIG.2 & FIG.10) to produce a voltage differential signal (COMP1/2 FIG.10, the 14->18 FIG.2); and the second stage (16 FIG.2) adjusts the voltage differential signal by the buffered voltage (18->16 FIG.2) to produce an output voltage (Rout FIG.11).

Allowable Subject Matter

5. Claims 9-10, 14-15, 20-21, 25-26, 30-31, 35-36, 46-47, 50-51, and 55-56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M Chang whose telephone number is 703-305-3416. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
February 27, 2004

CHIEH M. FAN
PRIMARY EXAMINER